HT1606

80-Segment Dot Matrix LCD Driver

Features

- Operating voltage:
  V_{DD}: 4.5~5.5V
  V_{EE}:-5~-23V
  V_{SS}=GND
- 80 internal LCD driver circuits
- 4-bit data format, bidirectional shift data transfer
- Standby mode to reduce power consumption
- 4.0MHz data transfer rate (CL2 input clock rate)
- Cascade connection interface

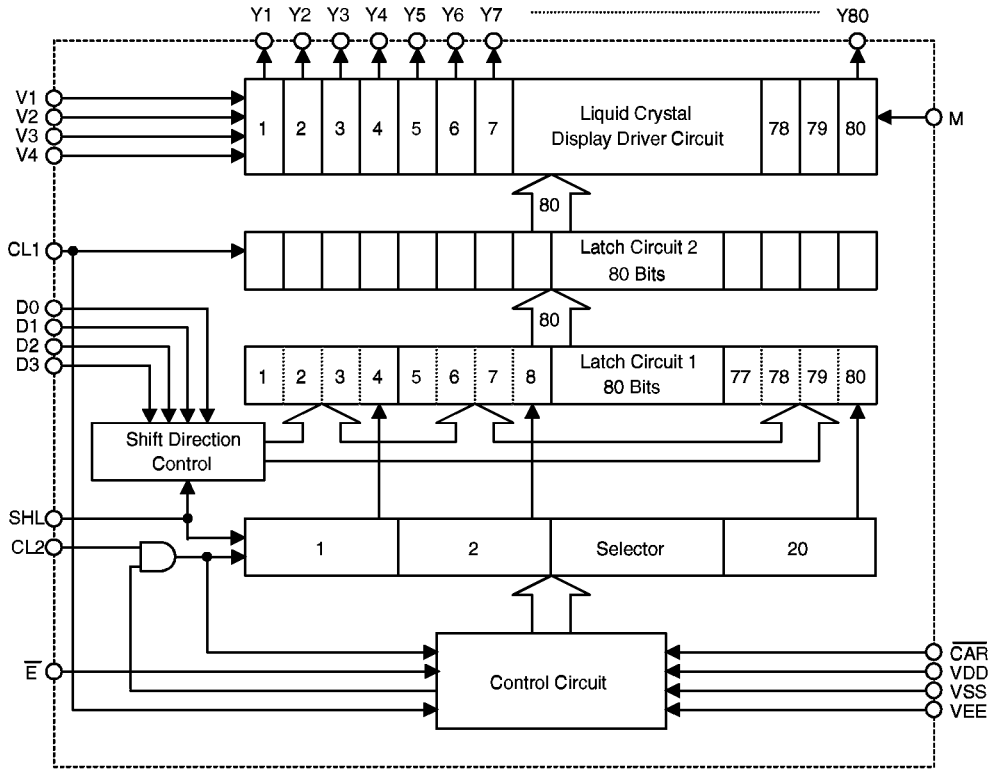
Applications

- Electronic dictionaries
- Portable computers
- Big LCD panels

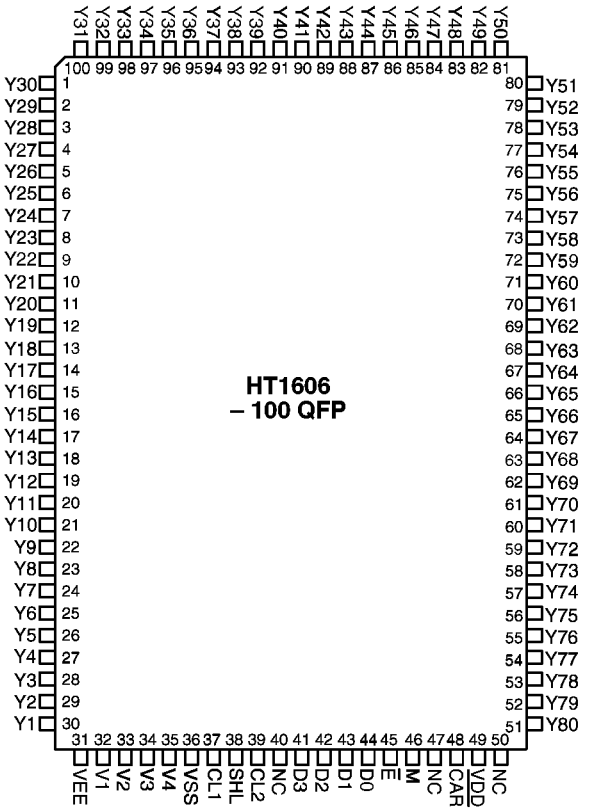
General Description

The HT1606 is an LCD segment driver designed for use in large area dot matrix liquid crystal graphic display systems. It provides 80 driver output lines. The high driving capacity can be used to drive a large screen. The HT1606 is fabricated in CMOS process. It is very suitable for use in portable battery drive equipments utilizing the liquid crystal display low power consumption. The chip can thus be applied to electrical dictionaries, portable computers, remote controllers, calculators, and other products with a large area LCD.

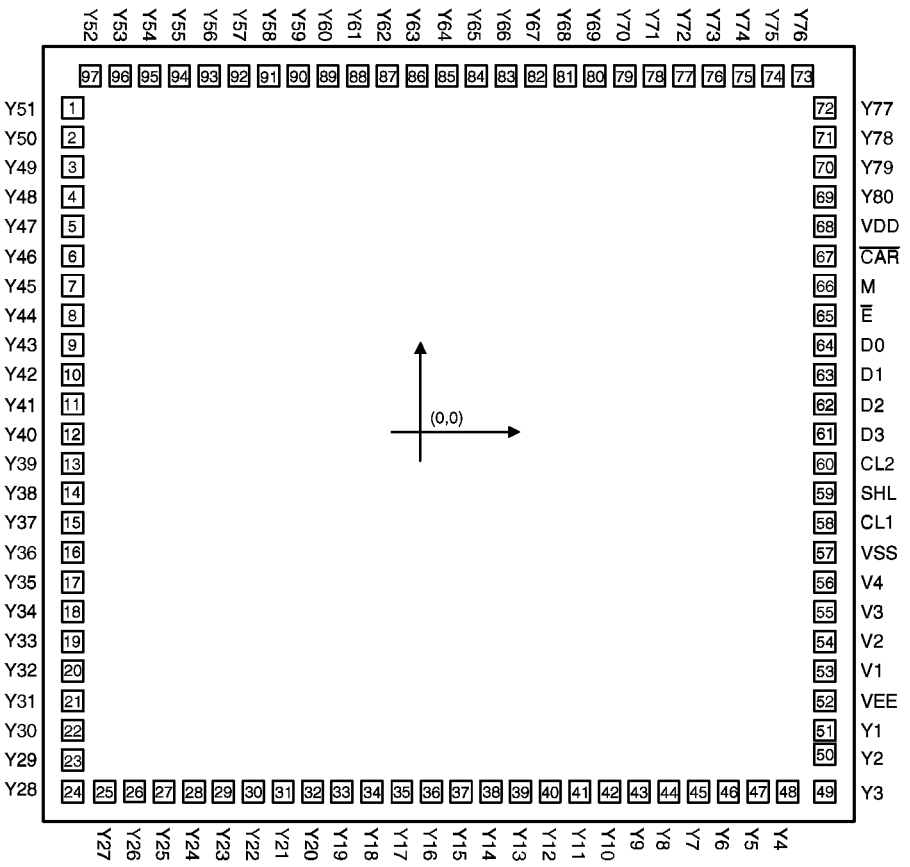
Block Diagram



Pin Assignment



Pad Assignment



Chip size: $4040 \times 3720\ (\mu m)^2$

* The IC Substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

Pad No.	X	Y	Pad No.	X	Y
1	–1895.0	1676.5	50	1895.0	–1509.5
2	–1895.0	1515.5	51	1895.0	–1369.5
3	–1895.0	1370.5	52	1895.0	–1229.5
4	–1895.0	1230.5	53	1895.0	–1084.5
5	–1895.0	1090.5	54	1895.0	–939.5
6	–1895.0	945.5	55	1895.0	–794.5
7	–1895.0	800.5	56	1895.0	–649.5
8	–1895.0	655.5	57	1895.0	–504.5

Pad No.	X	Y	Pad No.	X	Y
9	–1895.0	510.5	58	1895.0	–359.5
10	–1895.0	365.5	59	1895.0	–214.5
11	–1895.0	220.5	60	1895.0	–69.5
12	–1895.0	75.5	61	1895.0	75.5
13	–1895.0	–69.5	62	1895.0	220.5
14	–1895.0	–214.5	63	1895.0	365.5
15	–1895.0	–359.5	64	1895.0	510.5
16	–1895.0	–504.5	65	1895.0	655.5
17	–1895.0	–649.5	66	1895.0	800.5
18	–1895.0	–794.5	67	1895.0	945.5
19	–1895.0	–939.5	68	1895.0	1090.5
20	–1895.0	–1084.5	69	1895.0	1235.5
21	–1895.0	–1229.5	70	1895.0	1380.5
22	–1895.0	–1369.5	71	1895.0	1525.5
23	–1895.0	–1509.5	72	1895.0	1676.5
24	–1895.0	–1676.5	73	1734.5	1676.5
25	–1720.5	–1676.5	74	1589.5	1676.5
26	–1570.5	–1676.0	75	1444.5	1676.5
27	–1420.5	–1676.5	76	1299.5	1676.5
28	–1270.5	–1676.5	77	1154.5	1676.5
29	–1120.5	–1676.5	78	1009.5	1676.5
30	–970.5	–1676.5	79	864.5	1676.5
31	–820.5	–1676.5	80	719.5	1676.5
32	–670.5	–1676.5	81	574.5	1676.5
33	–520.5	–1676.5	82	429.5	1676.5
34	–370.5	–1676.5	83	284.5	1676.5
35	–220.5	–1676.5	84	139.5	1676.5
36	–70.5	–1676.5	85	–5.5	1676.5
37	79.5	–1676.5	86	–150.5	1676.5
38	229.5	–1676.5	87	–295.5	1676.5
39	379.5	–1676.5	88	–440.5	1676.5
40	529.5	–1676.5	89	–585.5	1676.5
41	679.5	–1676.5	90	–730.5	1676.5
42	829.5	–1676.5	91	–875.5	1676.5
43	979.5	–1676.5	92	–1020.5	1676.5
44	1129.5	–1676.5	93	–1165.5	1676.5
45	1279.5	–1676.5	94	–1310.5	1676.5
46	1429.5	–1676.5	95	–1455.5	1676.5
47	1579.5	–1676.5	96	–1600.5	1676.5
48	1729.5	–1676.5	97	–1745.5	1676.5
49	1895.0	–1676.5			

Pad Description

Pad No.	Pad Name	I/O	Function
1~51 69~97	Y51~Y1 Y80~Y52	O	LCD driver segment outputs
52, 57 68	VEE, VSS VDD	—	VDD-VSS : Power supply for internal logic VDD-VEE: Power supply for LCD driver circuit
53~56	V1~V4	I	Power supply for LCD driver V1 and V2 are selection levels V3 and V4 are non-selection levels
58	CL1	I	Latch clock input of display data The contents of the latch circuit 1 are latched into the latch circuit 2 on the falling edge of the CL1 signal.
59	SHL	I	Data shift direction control input
60	CL2	I	Data shift clock input for the shift register
61~64	D3~D0	I	Display data inputs
66	M	I	Input for converting the contents of the latch circuit 2 into AC waveform
65	$\overline{E}$	I	Chip enable control input
67	$\overline{CAR}$	O	Enable output for cascade connection A high to low transition on the CL1 not only sets $\overline{CAR}$ to "1" but resets the latch circuit addressing counter.

Absolute Maximum Ratings*

Supply voltage 1..... V_{SS}–0.3V~V_{SS}+5.5V

Supply voltage 2 ..... V_{DD}–28V~V_{DD}+0.3V

Input voltage 1** ..... V_{SS}–0.3V~V_{DD}+0.3V

Input voltage 2*** ..... V_{EE}–0.3V~V_{DD}+0.3V

Storage temperature ..... –50°C~125°C

Operating temperature ..... –25°C~75°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**: Applies to input terminals, SHL, CL1, CL2, D0~D3, $\overline{E}$ and M

***: Applies to V1, V2, V3 and V4, and must maintain
$V_{DD} \geq V1 \geq V3 \geq V4 \geq V2 \geq V_{EE}$
Connect a protection resistor of 15Ω ± 10% to each terminal in series

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage 1	—	—	4.5	5.0	5.5	V
V_{EE}	Operating Voltage 2	5V	—	–23	—	–5	V
I_{GND}	Operating Current 1	5V	No load*	—	—	2.0	mA
I_{EE}	Operating Current 2	5V	No load*	—	—	0.4	mA
I_{STB1}	Standby Current 1	5V	No load*	—	—	100	μA
I_{STB2}	Standby Current 2	5V	No load**	—	—	1	μA
V_{IH}	Input High Voltage	5V	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Input Low Voltage	5V	—	0	—	$0.3V_{DD}$	V
I_{OH}	Output Source Current	5V	V_{OH}=4.5V	0.5	—	—	mA
I_{OL}	Output Sink Current	5V	V_{OL}=0.5V	0.5	—	—	mA
R_{ON}	Driver ON Resistance Y1~Y80	5V	V_{EE}=-10V Load current =100μA	—	—	7.5	kΩ
I_{IL1}	Input Leakage 1	5V	V_{IN}= 0 to V_{DD}	–1	—	1	μA
I_{IL2}	Input Leakage 2	5V	V_{IN}= V_{EE} to V_{DD}	–25	—	25	μA
t_{CL2}	CL2 Cycle Time	5V	—	250	—	—	ns

*: The testing conditions are listed below:
f_{CL1}=16kHz
f_{CL2}=4MHz
f_M=30Hz
I_{GND}: currents between V_{DD} and GND
I_{EE}: currents between V_{DD} and V_{EE}
I_{STB1}: currents between V_{DD} and GND and $\overline{E}$="1"

**: $f_{CL1}=f_{CL2}=f_M$=0Hz

Functional Description

Selector circuit

The selector circuit consists of an up-down addressing counter and an encoder circuit. The addressing counter addresses the latch circuit through an address encoder. The transferred data is written into the corresponding latch addressed by the addressing counter.

Shift direction control circuit

The shift control circuit controls the shift direction of transferred data. The data bus is of 4 bits wide. The direction of data transfer can be set to left or right by the SHL signal. When the SHL signal is "0" the addressing counter shifts left; otherwise the counter shifts right. The addressing counter always shifts on the falling edge of the shift clock CL2, and the display data are input from the D0~D3 pins.

When the SHL signal is "0", the input data D0~D3 are latched into the 4N+4 ~ 4N+1 latches of the latch circuit 1, where the value of N ranges from 0 to 19 and is controlled by the addressing counter. On the other hand, when the SHL signal is "1", the input data D0~D3 are latched into the 4N+1 ~ 4N+4 latches of the latch circuit 1, where the value of N ranges from 19 to 0. The following table illustrates the relationship of the SHL level, shift direction, and data pins (D0~D3).

SHL	Shift Direction and Data Mapping
0	D3 -> 1 -> 5 -> --- -> 73 -> 77
	D2 -> 2 -> 6 -> --- -> 74 -> 78
	D1 -> 3 -> 7 -> --- -> 75 -> 79
	D0 -> 4 -> 8 -> --- -> 76 -> 80
1	D3 -> 80 -> 76 -> --- -> 8 -> 4
	D2 -> 79 -> 75 -> --- -> 7 -> 3
	D1 -> 78 -> 74 -> --- -> 6 -> 2
	D0 -> 77 -> 73 -> --- -> 5 -> 1

Standby mode

The HT1606 enters the standby mode to reduce power consumption when the $\overline{E}$ input is high. In the standby mode the $\overline{CL2}$ and D0~D3 pins are all inhibited. But the $\overline{CAR}$ pin has to acknowledge that data transfer is completed. The $\overline{CAR}$ pin can be connected to the $\overline{E}$ pin of the next chip for cascade connection applications. Once the data transfer of the prior chip is completed, the $\overline{CAR}$ signal will wake up the next chip, and then the next chip will begin to receive data. The $\overline{CAR}$ and $\overline{E}$ signals are important for cascade connection applications.

Latch circuit

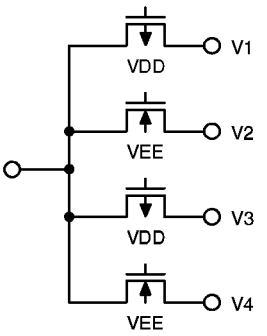
There are two latch circuits, i.e., 20 × 4-bit latch circuit 1, and 80 × 1-bit latch circuit 2. The latch circuit 1 is of 4 bits wide and designed for high speed data transfer. The selector circuit allows only one 4-bit data to change at a time since it is very useful for power saving in the high speed data transfer. Once the data transfer of latch circuit 1 is completed, the data to be displayed on the latch circuit 1 are latched into the latch circuit 2 on the falling edge of the CL1 signal. After the data transfer between the latch circuit 1 and latch circuit 2 is completed, the addressing counter will reset (on the falling edge of the CL1 signal) and the latch circuit 1 will receive new data for the next segment display. The CL1 signal can be used to synchronize data output of all connected chips for cascade connection applications. When the data transfer of all chips to the latch circuit 1 is completed, the CL1 input changes from high to low so as to latch all data on the latch circuit 1 into the latch circuit 2 for output synchronization.

LCD driver circuit

The LCD driver circuit outputs the selected level to drive an external LCD panel. The selected level is decided by the M signal and the data on the latch circuit 2. The combination of data (D) from the latch circuit 2 with the M signal allows one of the 4 liquid crystal display driver levels V1, V2, V3, and V4 to be transferred to the output lines (Y1~Y80). The relationship of the output level, M and, D is as listed.

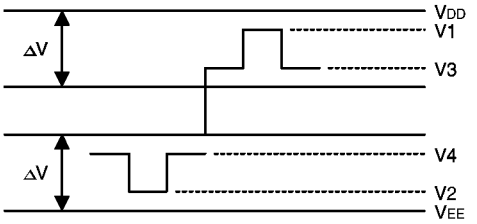
M	1	1	0	0
D	1	0	1	0
Output Level	V1	V3	V2	V4

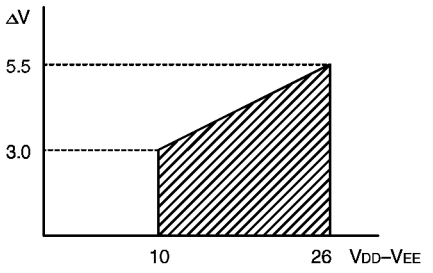
The configuration of the LCD driver segment output is as shown.



LCD driver power supply – V1, V2, V3, V4

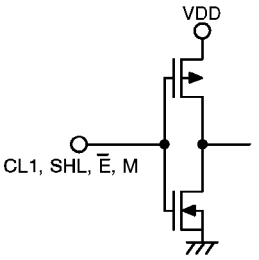
The HT1606 requires four external voltage sources to support the internal LCD drive power levels. Apply the positive voltage to V1 and V3 and the negative voltage to V2 and V4 within the ΔV range. The impedance on driver output is stable. The value of ΔV depends on the power supply voltage VDD-VEE. The following diagrams illustrate the ΔV definition and relationship between VDD-VEE and ΔV.



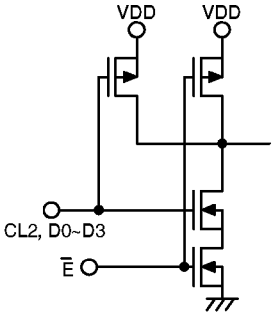


I/O Pin configurations

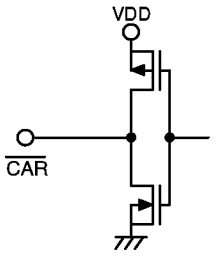
- The configurations of the CL1, SHL, E and M input pins are identical as shown.



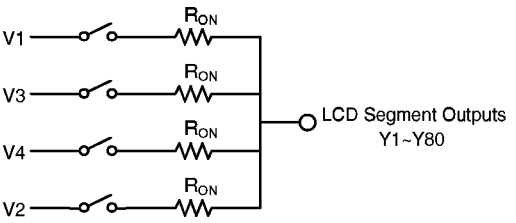
- The configurations of the CL2 and D0~D3 input pins are all identical as shown.



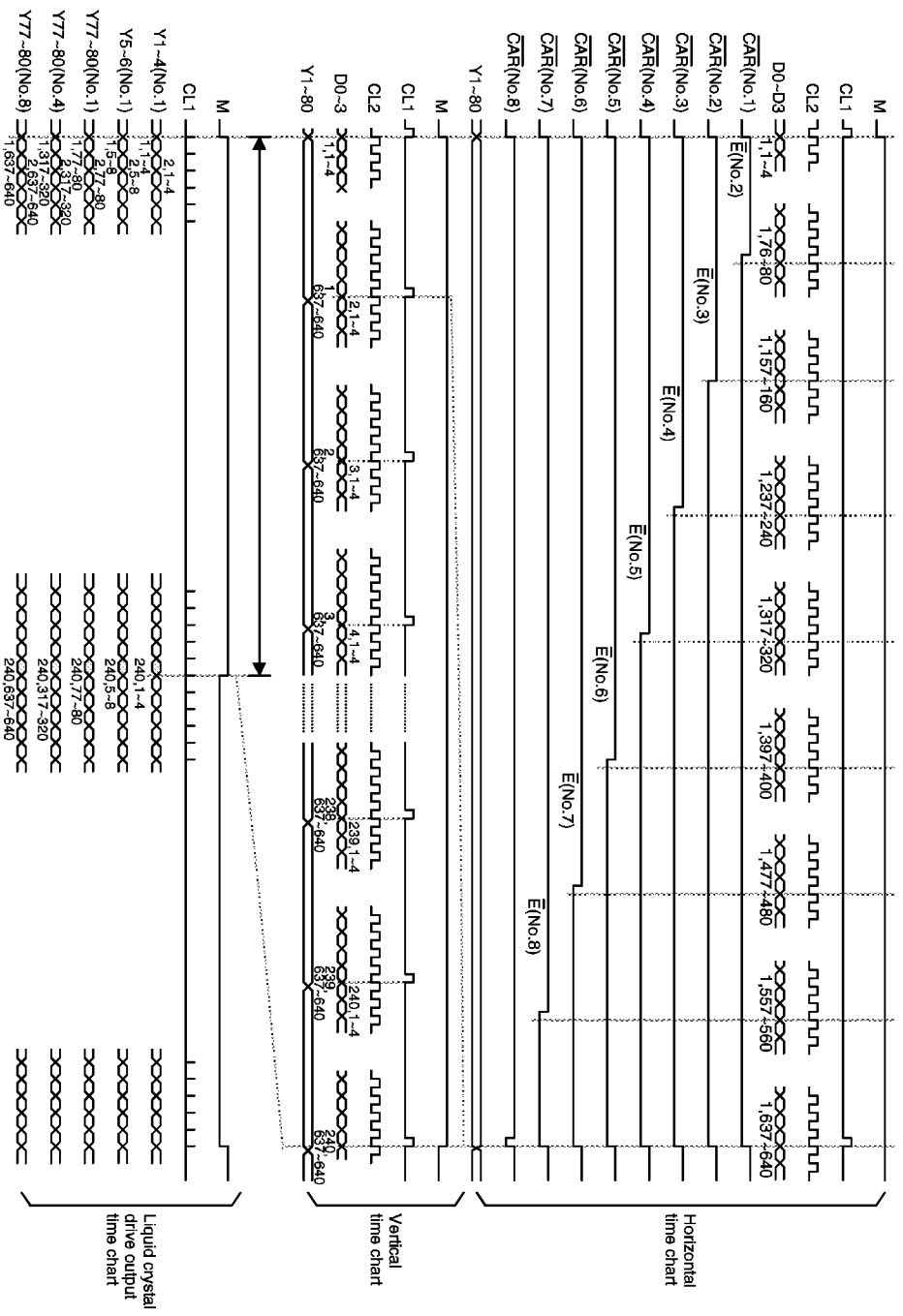
- The configuration of the output pin CAR is as shown.



- The configurations of Y1~Y80 output pins are the same as shown.



Example of Waveform



Application Circuits

The following is an LCD panel with 240 × 640 dots. The characters are displayed with 1/240 duty dynamic drive on the LCD panel.